【Claims】

【Claim 1】 A method for fabricating a semiconductor device, comprising the steps of:

forming a hard mask insulation layer on an etch target layer;

forming a hard mask sacrificial layer on the hard mask insulation layer;

coating a photoresist on the hard mask insulation layer;

selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern;

selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width;

removing the photoresist pattern;

etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width; and

etching the etch target layer by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width, wherein the first width is wider than the fourth width by at least about 20 nm.

【Claim 2】 The method as recited in claim 1, wherein the etch

target layer is a conductive layer and the line pattern is one of a bit line, a word line and a metal line.

【Claim 3】 The method as recited in claim 1, wherein the photoresist is one of a photoresist for use in ArF photolithography and a photoresist for use in F_2 photolithography.

【Claim 4】 The method as recited in claim 1, wherein magnitudes of the first width to the fourth width are in a descending order of the first width, the second width, the third width and the fourth width.

【Claim 5】 The method as recited in claim 1, wherein the sacrificial hard mask is removed at the step of removing the etch target layer.

【Claim 6】 The method as recited in claim 1, wherein the hard mask sacrificial layer is made of a material selected from a group consisting of polysilicon, aluminum (Al), tungsten (W), tungsten silicide (WSi_x), where x ranges from about 1 to about 2, tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), titanium silicide ($Tisi_x$), where x ranges from about 1 to 2, titanium aluminum nitride (TiAlN), titanium silicide nitride (TiSiN), platinum (Pt), iridium (Ir), iridium oxide (IrO_2), ruthenium (Ru), ruthenium oxide (RuO_2),

silver (Ag), gold (Au), cobalt (Co), tantalum nitride (TaN), chromium nitride (CrN), cobalt nitride (CoN), molybdenum nitride (MoN), molybdenum silicide ($MoSi_x$), where x ranges from about 1 to about 2, aluminum oxide (Al_2O_3), aluminum nitride (AlN), Platinum silicide ($PtSi_x$), where x ranges from about 1 to about 2, and chromium silicide ($CrSi_x$), where x ranges from about 1 to 2.

【Claim 7】 The method as recited in claim 6, wherein the etch target layer is made of the same material used for the hard mask sacrificial layer.

【Claim 8】 The method as recited in claim 1 or 6, wherein the hard mask sacrificial layer is formed by using one of an oxide-based material and a nitride-based material.

【Claim 9】 The method as recited in claim 6, wherein at the step of etching the hard mask sacrificial layer, a plasma containing a mixed gas of sulfur hexafluoride (SF_6) and nitrogen (N_2) is used if the hard mask sacrificial layer is made of tungsten.

【Claim 10】 The method as recited in claim 9, wherein at the step of etching the hard mask sacrificial layer made of tungsten, bottom and top portions of a reaction chamber of a reactive ion etching (RIE) apparatus are supplied with

different powers ranging from about 450 Watt to about 850 Watt and from about 30 Watt to about 60 Watt, respectively along with a chamber pressure maintained in a range from about 8 mTorr to about 16 mTorr and a mixed gas of SF_6 and N_2 each with a quantity in a range from about 7 sccm to about 13 sccm and from about 10 sccm to about 20 sccm, respectively.

【Claim 11】 The method as recited in claim 6, wherein at the step of etching the hard mask sacrificial layer, a chlorine-based gas is used as a main etch gas if the hard mask sacrificial layer is formed with one material of polysilicon and Ti and one of oxygen (O_2) gas and carbon fluoride (CF) gas is added to the main etch gas to control an etch profile.

【Claim 12】 The method as recited in claim 6, wherein at the step of etching the hard mask sacrificial layer, one of a chlorine-based plasma and a fluorine-based plasma is used if the hard mask sacrificial layer is made of a material selected from a group consisting of Pt, Ir, Ru and any one oxidated material of these listed metals.

【Claim 13】 The method as recited in claim 8, wherein at the step of etching the hard mask insulation layer, a plasma containing a mixed gas of carbon tetrafluoride (CF4), trifluoro methane (CHF_3), argon (Ar) and oxygen (O_2) is used if the hard mask insulation layer is made of a nitride-based

material.

【Claim 14】 The method as recited in claim 13, wherein at the step of etching the nitride-based hard mask insulation layer, a RIE apparatus is used by supplying a power in a range from about 400 Watt to about 800 Watt along with a pressure maintained in a range from about 35 mTorr to about 65 mTorr and a mixed gas of CF_4, CHF_3, Ar and O_2 each with a quantity in a range from about 25 sccm to about 65 sccm, from about 40 sccm to about 80 sccm, from about 50 sccm to about 100 sccm and from about 12 sccm to about 25 sccm, respectively.

【Claim 15】 The method as recited in claim 2 or 5, wherein the etch target layer includes tungsten and at the step of etching the etch target layer, the etching proceeds by using a plasma containing a mixed gas of SF_6 and N_2.

【Claim 16】 A method for fabricating a semiconductor device, comprising the steps of:

forming a hard mask insulation layer on an etch target layer;

forming a hard mask sacrificial layer on the hard mask insulation layer;

forming an anti-reflective coating layer on the hard mask sacrificial layer;

coating a photoresist on the anti-reflective coating

layer;

selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern;

etching the anti-reflective coating layer by using the photoresist pattern as an etch mask;

selectively etching the hard mask sacrificial layer with use of the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width;

removing the photoresist pattern and the anti-reflective coating layer;

etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width; and

etching the etch target layer by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width, wherein the first width is wider than the fourth width by at least about 20 nm.

【Claim 17】The method as recited in claim 16, wherein the photoresist is one of a photoresist for use in ArF photolithography and a photoresist for use in F_2 photolithography.

【Claim 18】The method as recited in claim 16, wherein magnitudes of the first width to the fourth width are in a

descending order of the first width, the second width, the third width and the fourth width.

【Claim 19】 The method as recited in claim 16, wherein the hard mask sacrificial layer is made of a material selected from a group consisting of polysilicon, Al, W, WSi_x, where x ranges from about 1 to about 2, WN, Ti, TiN, $TiSi_x$, where x ranges from about 1 to 2, TiAlN, TiSiN, Pt, Ir, IrO_2, Ru, RuO_2, Ag, Au, Co, TaN, CrN, CoN, MoN, $MoSi_x$, where x ranges from about 1 to about 2, Al_2O_3, AlN, $PtSi_x$, where x ranges from about 1 to about 2 and $CrSi_x$, where x ranges from about 1 to 2.

【Claim 20】 The method as recited in claim 16, wherein the anti-reflective coating layer is made of an organic material.

【Claim 21】 The method as recited in claim 18, wherein the step of etching the anti-reflective coating layer proceeds by using a plasma containing a mixed gas of Cl_2 and Ar.

【Claim 22】 The method as recited in claim 21, wherein at the step of etching the anti-reflective coating layer, bottom and top portions of a reaction chamber of a RIE apparatus are supplied with different powers ranging from about 400 Watt to about 800 Watt and from about 70 Watt to about 130 Watt, respectively along with a chamber pressure maintained in a

range from about 6 mTorr to about 12 mTorr and a mixed gas of Cl_2 and Ar each with a quantity in a range from about 35 sccm to about 65 sccm and from about 20 sccm to about 50 sccm, respectively.

【Claim 23】 A method for fabricating a semiconductor device, comprising the steps of:

forming a conductive layer containing tungsten on a substrate;

forming a hard mask insulation layer on the conductive layer;

forming a hard mask sacrificial layer containing tungsten on the hard mask insulation layer;

forming a photoresist pattern having a first width on the hard mask sacrificial layer to form a line pattern;

selectively etching the hard mask sacrificial layer with use of the photoresist pattern as an etch mask to form a sacrificial hard mask having a second with;

removing the photoresist pattern;

etching the hard mask insulation layer with use of the sacrificial hard mask as an etch mask by controlling excessive etching conditions to thereby form a hard mask having a third width; and

etching the conductive layer by using the sacrificial hard mask and the hard mask as an etch mask to form a line type conductive pattern having a fourth width, wherein the first width is wider than the fourth width by at least about

20 nm.

【Claim 24】The method as recited in claim 23, wherein the photoresist pattern is one of a photoresist for use in ArF photolithography or a photoresist for use in F_2 photolithography.

【Claim 25】The method as recited in claim 23, wherein the conductive pattern is one of a bit line, a word line and a metal line.

【Claim 26】The method as recited in claim 23, wherein magnitudes of the first width to the fourth width are in a descending order of the first width, the second width, the third width and the fourth width.

【Claim 27】The method as recited in claim 23, wherein the sacrificial hard mask is removed at the step of etching the conductive layer.

【Claim 28】The method as recited in claim 23, wherein the conductive layer is made of the same material used for forming the hard mask sacrificial layer.

【Claim 29】The method as recited in claim 23 or 28, wherein the conductive layer and the hard mask sacrificial layer both

containing tungsten include any one of a W layer, a WSi_x layer and WN layer.

【Claim 30】 The method as recited in claim 23 or 28, wherein the hard mask insulation layer is formed with one of an oxide-based material and a nitride-based material.

【Claim 31】 The method as recited in claim 23, further including the step of forming an anti-reflective coating layer on between the hard mask insulation layer and the hard mask sacrificial layer.

【Claim 32】 The method as recited in claim 23, wherein the step of etching the hard mask sacrificial layer proceeds at a RIE apparatus by using a plasma containing a mixed gas of SF_6 and N_2 and top and bottom portions of a reaction chamber of the RIE apparatus are supplied with different powers ranging from about 450 Watt to about 850 Watt and from about 30 Watt to about 60 Watt, respectively along with a pressure maintained in a range from about 8 mTorr to about 16 mTorr, SF_6 with a quantity ranging from about 7 sccm to about 13 sccm and N_2 with a quantity ranging from about 10 sccm to about 20 sccm.